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AN INVESTIGATION OF POTENTIAL APPLICATIONS OF
OP-SAPs - OPERATIONAL SAMPLED ANALOG PROCESSORS

Semi-Annual Report

Grant No. NSG-1223

Submitted to:

NASA Scientific & Technical Information Facility
P. O. Box 8757
Baltimore/Washington International Airport
Maryland 21240

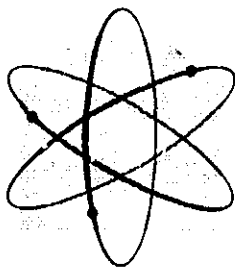
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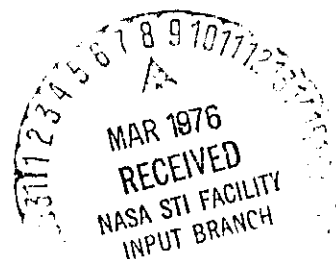
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INTRODUCTION

The research described herein is directed at a long-term investigation of the impact that charge-coupled device (CCD) processors portend for future instrumentation. The CCD devices of interest process sampled analog data and will be referred to in the sequel as OP-SAPS - operational sampled analog processors.

Preliminary studies into various architectural configurations for systems composed of OP-SAPS have shown that they enjoy tremendous potential in such diverse applications as pattern recognition [1] and automatic control [2]. In addition, it appears probable that OP-SAPS may be used to construct computing structures which can serve as special peripherals to large-scale computer complexes used in real time flight simulation [3].

Because of the inherent advantages OP-SAPS possess for computations of the form found very often in pattern recognition and image processing systems, the scope of the research has been limited to the following benchmark programs: (1) Face Recognition, (2) Voice Command and Control, (3) Terrain Classification, and (4) Terrain Identification. Of these four, only the first two have received significant attention to this point. A small amount of effort has been spent on examining a method by which OP-SAPS may be used to decrease the limiting ground sampling distance encountered in remote sensing from satellites.

1. FACE IDENTIFICATION PROGRAM

This problem area involves the development of a pattern recognition system for facial identification. There is a large variety of applications for such a system, including control of access to secure areas, personnel identification/verification, etc.

The initial system is designed to handle fifty different faces. This constraint was imposed to limit the amount of data gathering prior to establishing feasibility. The steps to be followed are:

- a. Establish a statistically meaningful data base
- b. Design feature extractor
- c. Design classifier
- d. Test on independent data, using digital computers
- e. Iterate on steps b - d as required
- f. Design CCD hardware
- g. Implementation

At this point in time, steps a and b are being carried out. Computer software and hardware are available to allow acquisition of facial information through a standard vidicon camera. The raw data is acquired at a sampling rate of 200 KHz, and each sample point is quantized to 8 bits. An analysis will be carried out to determine the composite power density spectrum from which the bandwidth for a pre-filter and the minimum sampling rate will be estimated. The resulting system will be as shown in Figure 1.

Once the required sampling rate has been determined, the next step involves the design of the feature extractor. The purpose of the feature extractor is to make meaningful measurements on the input samples which are as few in number as possible consistent with satisfactory performance. This step is generally viewed as performing dimensionality reduction, since the number of features is normally small relative to the original number of samples.

Since CCD processors are well suited to perform linear transformations, the feature extractor and classifier will be constrained to such techniques.

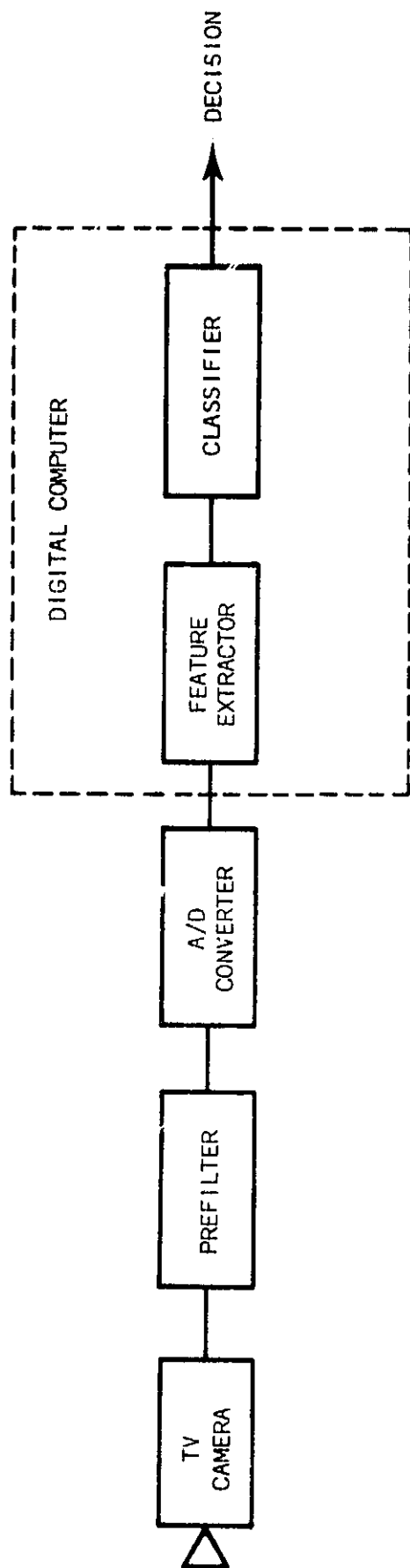


Figure 1 Block diagram of digital implementation

At present, it is planned to use a version of the feature extractor defined and patented by Object Recognition Systems, Incorporated.* In essence, this is a variation of scanning through an optical slit in that the time sequence obtained from sampling a field of the TV raster is divided into a number of intervals over which integration operations are performed. The result from each interval is used as a feature, and the total number of intervals determines the resulting dimensionality of the feature vector.

Preliminary testing of this feature extractor has been encouraging; and, therefore, work will continue in an effort to determine an optimum number of features. At present, it appears that this number will lie between 10 and 32, which is compatible with planned CCD structures.

2. VOICE COMMAND AND CONTROL SYSTEM

An investigation on the feasibility of a voice-actuated command and control system using CCD processors is being conducted. The result is to be a system which is capable of recognizing words or phrases spoken by an operator for whom it has been previously trained.

The potential for performing fast and complex processing of speech signals with CCD's has generated interest in the possibility of using such a voice-actuated system for aviation. Such a system could perform simple tasks as responding to vocal requests about altitude, range, speed, etc.

The investigation has been broken into two phases. The first phase is the study and simulation on a minicomputer of a speech processing technique which could be applicable to CCD implementation. The second phase is the actual CCD implementation of the system. The initial work has included the collection of information on the characteristics of speech and speech processing. Also computer simulation of some of the theory has been conducted.

* Since the scope of this research is limited to applications of OP-SAPS to solve pattern recognition problems, we are not doing extensive work in feature extraction theory. Hence, an existing algorithm was chosen.

Initial literature study and experiments led to the conclusion that better results might be obtained if feature measurements from an utterance were made in the frequency domain rather than in the time domain. In order to eliminate phase shift problems such as created by the detection of the beginning of an utterance, the frequency information is presented as the power density spectrum. This concept is compatible with the use of existing laboratory CCD Fourier transform devices.

The problem now arises as to how much and what type information is necessary for correct classification. It is fairly widely accepted that systems for speech recognition can be band-limited to around 4 KHz, thereby requiring at least an 8 KHz sampling rate. It was also determined that a one second interval is sufficient for most utterances of initial interest. These requirements then dictate the processing of 8000 samples per utterance. In order to accomodate this amount of data with present CCD technology, the interval must be broken into sub-intervals. The size of each sub-interval is purely a function of how much frequency resolution is necessary for correct classification. The power density spectrum for each sub-interval is then used to obtain an average power density spectrum or periodogram for the entire utterance. Example periodograms for the words "ON" and "OFF" are shown in Figures 2 and 3, respectively. The sub-interval in each of these examples was 512 samples wide and the sampling interval contained 16 sub-intervals. With the sampling interval approximately one second long, each sub-interval contains 62.5 milliseconds of speech and the periodogram has a resolution of 16 Hz.

It should be noted that although the amplitude of each power density spectrum is down 20 db or more after approximately 1500 Hz, certain characteristics of speech in the frequency band from 1500 to 3000 Hz may be necessary for the discrimination of certain utterances.

The next step is to select a feature extraction scheme for use with the periodograms. One scheme which was implemented was that of dividing the periodogram into bands from which the total energy in each band is calculated and considered as a feature. Results using a minimum distance classifier with this feature vector produced promising but not yet satisfactory results.

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

0db
-3db
-10db
-20db

POWER (NORMALIZED)

0 1000 2000 3000 4000

FREQUENCY (HZ)

Figure 2 Power density spectrum of "on"

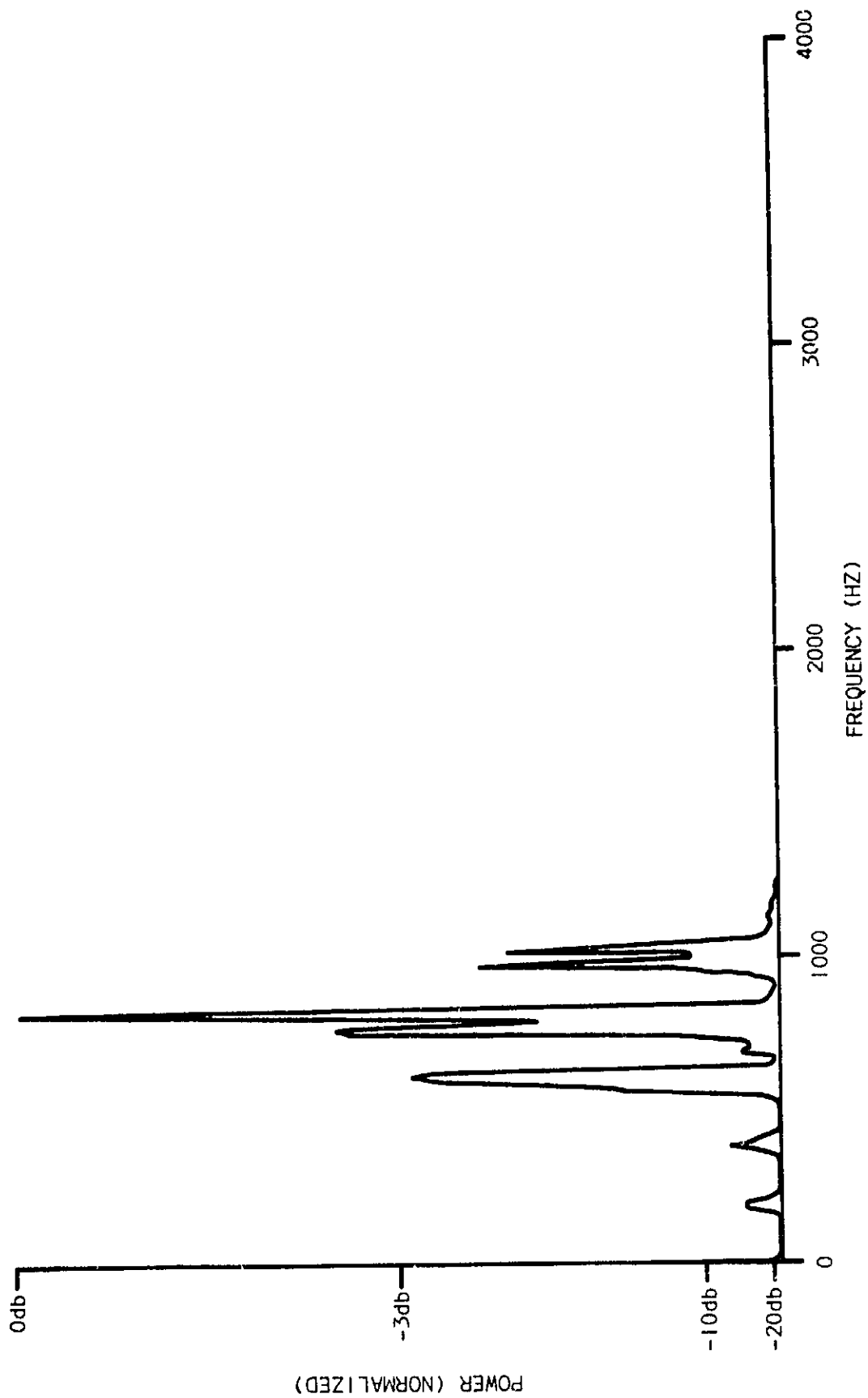


Figure 3 Power density spectrum of "off"

Variations on the feature extraction technique along with other configurations for speech processing using CCD's are being investigated. It is felt that CCD's can play an important role in speech recognition systems.

3. THEORETICAL STUDY OF A CCD PROCESSOR TO CONVERT GREY LEVEL INFORMATION TO BLACK AND WHITE INFORMATION

Prior research was conducted by the authors at a low level of funding for four years under sponsorship of the Air Force Office of Scientific Research on the conversion of grey level information to black and white information. Support stopped approximately one year ago but work has continued in the form of a Ph. D. dissertation that is being completed on a nonfunded basis.

We have shown [4] that information from grey level sensors of a particular size may be converted into black and white information which would be produced by sensors much smaller than the grey level sensors. In effect, the resolution has been enhanced. Theoretical examples have been worked which indicate an increase in resolution of 4 to 1 [5]. The limiting conditions have not been established but system complexity increases as resolution enhancement increases. It appears possible that CCD's could be used for the signal processing because of the type of data processing to be done and because a means is needed for processing a large amount of data at high speed. Such processing may lead to techniques whereby the ground sampling distance achievable with remote sensing may be decreased.

The basic model of the system results in a non-square matrix which needs to be inverted to obtain design equations. Of course, a non-square matrix cannot be inverted, but a pseudo-inverse does exist and it has been used [6]. Results by Jain and Angle [7] on similar modeling suggests a solution to the design problem using the fast Fourier transform.

Present efforts are involved in interpreting a Jain and Angle type model in terms of CCD implementable functions. The goal is to design a CCD system for an example problem and predict its performance. The cost of conventional hardware in terms of size, power consumption, etc., compared to CCD cost factors will be of special concern in the work.

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